IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#17/D
1/25/01

In re CPA of:

Possley

Examiner: N. Ngo

Application No.: 09/262,458

Art Unit: 2814

Filed: March 4, 1999

For: Gate Array Architecture

AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Dear Sir:

For the above continued prosecution application (CPA), please enter the following amendments and consider the following remarks:

IN THE CLAIMS:

(Twice amended) 1. An integrated circuit comprising: a gate array architecture;

said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites[**to form**], **at least one forming both** N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors;

successive rows of small diffusion regions are followed by successive rows of regular sized diffusion regions; and

immediately successive rows within similarly-sized diffusion regions have opposite polarity.